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Hardware
Documentation

Data Sheet

HVC 5222C-B2

1 A Motor Controller for BLDC or BDC Motors with 32 KB Flash and LIN

Smart|HVC Technology

easy|LIN® Technology

ARM Powered®

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1 A Motor Controller for BLDC or BDC Motors with 32 KB Flash and LIN

Release Note: Revision bars indicate significant changes to the previous edition.

1. Introduction

The HVC 5222C is an automotive qualified, fully integrated motor controller for BLDC or BDC motor applications. The IC integrates three half-bridges, driving up to 1 A each, with an Arm® Cortex®-M3 CPU, 32 KB flash memory and many analog and digital motor specific functions to enable:

– Sensored and sensor-less control of a single BLDC motor.

– H-bridge control of up to two BDC motors.

An auto-addressing capable LIN transceiver allows for external bus control of the application. Seven general-purpose I/O pins and a 15 mA, 3.3 V supply help integrate sensors, switches, LEDs, or other local functions into the application. All of these features combined with many automotive diagnostic and protection mechanisms, in a compact 5×5 mm^2 24-pin QFN package make the HVC 5222C a suitable solution for compact automotive actuator applications.

Table 1–1: Version Overview

Ordering Number	Flash	SRAM	Motor Terminals	Package
HVC 5222C-B2	32 KB	2 KB	3 × 1 A peak	PQFN 24

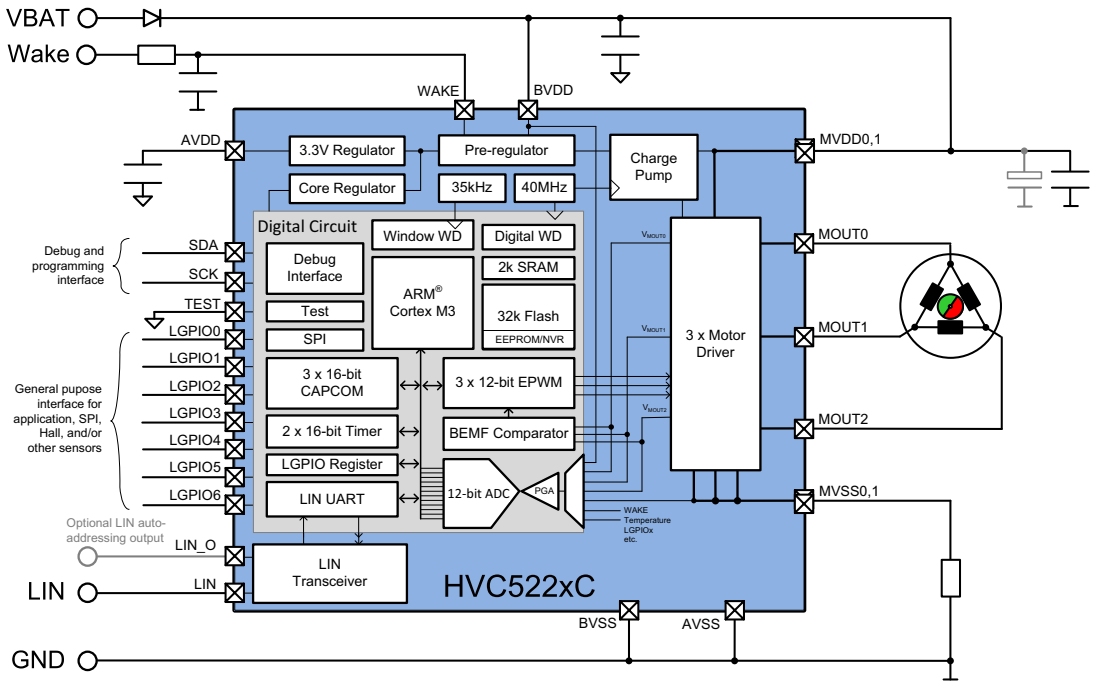


Fig. 1–1: Typical application diagram for a BLDC motor.

1.1. Features

Table 1–2 gives an overview of the features of the HVC 5222C devices.

Table 1–2: HVC 5222C feature list

Item	Feature	
Power System		
Supply Voltage Range	Parameters guaranteed from 6 V to 18 V, functional to 28 V.	
	Transient from 4.5 V to 40 V without motor operation.	
3.3 V Regulator	3.3 V for external loads up to 15 mA total, including LGPIO loads.	
Supply supervision	BVDD over- and undervoltage interrupt.	
	Analog monitoring via ADC at pins BVDD and/or WAKE.	
Motor Interface and Control		
Motor Bridge	**HVC 5222C**	Three 1 A(peak) half-bridge drivers
Current Sensing	Motor-current sensing with one external shunt resistor.	
Protection	Overcurrent, overvoltage, and overtemperature protection.	
PWM Generation	12-bit Enhanced PWM (EPWM) module supporting center- or edge aligned PWM generation.	
BEMF Comparators	Phase comparator zero crossing detection against an integrated virtual star point resistor network.	
Measurement System	12-bit ADC with 1 µs conversion time and various trigger options: • BVDD supply voltage • 3 MOUT ports • WAKE port • Current sensing with external shunt resistor • All LGPIOx analog voltages • LGPIO5/6 differential voltage • LIN bus-shunt voltage • Linear die temperature	
External Sensor Interface	Analog, CAPCOM or SPI via 7 general-purpose IOs.	
Microcontroller		
CPU	Arm® Cortex®-M3	
CPU clock (f_{CPU})	Up to 20 MHz with optional EMI reduction module (ERM).	
Interrupt Controller	NVIC with 19 interrupt lines and 8 priority levels.	
Debug Interface	Serial wire debug interface via SDA and SCK inputs.	
CPU Reset	Software reset and optional external reset input via SDA pin.	

Table 1–2: HVC 5222C feature list**, continued**

Item	Feature
Memory	
Flash	32 KB (8192 x 32-bit) with error correction.
RAM	2 KB (512 x 32-bit).
Startup ROM	1 KB (includes flash-utility routines for erase and write).
EEPROM	512 byte (128 x 32-bit) with error correction.
NVR	256 byte (64 x 32-bit) with error correction.
Digital Periphery	
System Clocks	40 MHz main oscillator with spread-spectrum (ERM) option.
	35 kHz auxiliary oscillator.
Clock Supervision	Digital watchdog clocked with 20 MHz system clock.
	Window watchdog clocked with a 35 kHz auxiliary oscillator.
Timers and Counters	24-bit SysTick Timer.
	CAPCOM unit with 3 channels.
	Two 16-bit timers usable as timer, counter, capture input, output compare or PWM output.
Communication	LIN-UART with automatic baud rate adjustment and receive/transmit FIFOs.
	SPI module (Master only).
Input and output	
Wake from Sleep	Via LIN or WAKE pin.
General-Purpose IOs	7 × digital I/O (push-pull or open-drain mode). Usable as single-ended analog input. LGPIO5 and LGPIO6 as differential analog input.
Vehicle Interface	LIN ISO17987/SAE2602 compliant transceiver supporting auto-addressing via the bus-shunt method (BSM).

2. Package and Pins

2.1. Pin Assignment

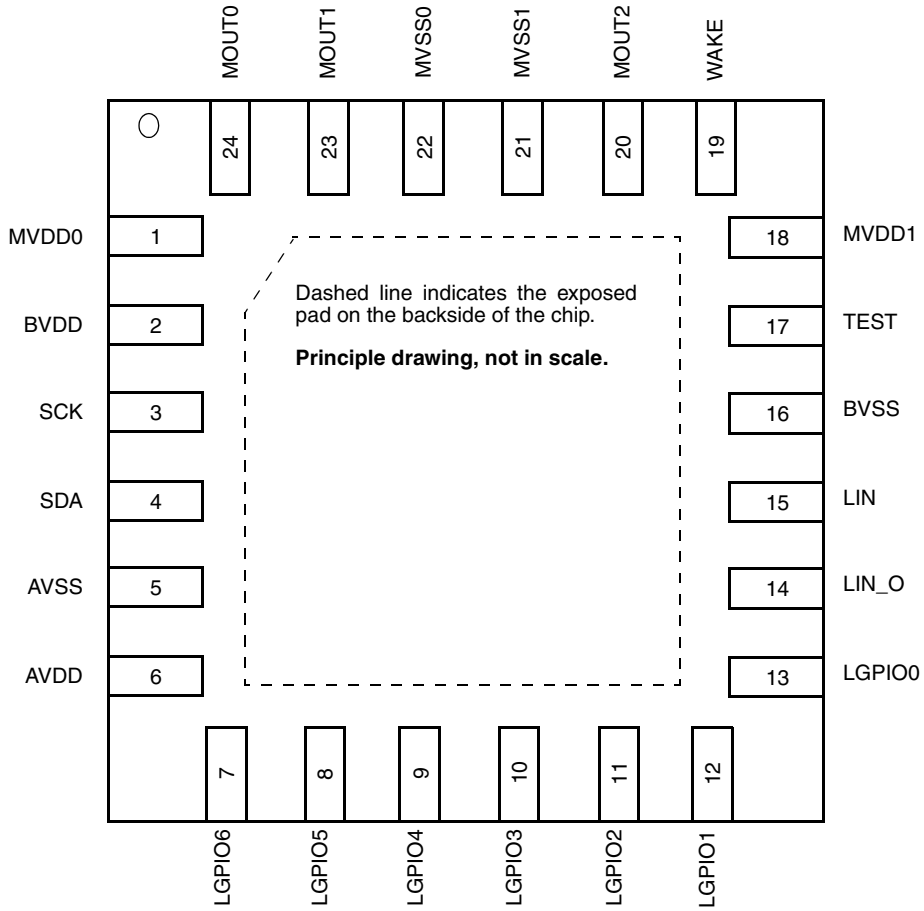


Fig. 2–1: Pin assignment of the HVC 5222C in PQFN24 package (Top View)

2.2. Pin List

Table 2–1: Pin List

No.	Name	Type[1)]	Module / Function
1	MVDD0	HV S	DC-link voltage for the motor and power supply pin of internal half-bridges. Must be connected to BVDD and MVDD1. Requires C_{MVDD} capacitance to BVSS depending on application and motor use.
2	BVDD	HV S	System supply, must be protected against reverse polarity and bypassed to BVSS by C_{BVDD} close to the IC. Chip supply and motor voltage measurement via the ADC.
3	SCK	Dig. In	Debug interface clock (in application mode the pin can be left open due to the internal weak pull-down resistor).
4	SDA	Dig. I/O	Debug interface data (in application mode the pin can be left open due to the internal weak pull-up resistor). Also configurable as an external active-low reset input.
5	AVSS	G	Analog ground. Internally connected to BVSS with anti-parallel diodes. Must be connected to BVSS on the PCB.
6	AVDD	P	3.3V Output of the internal AVDD regulator and digital interface voltage. Must be buffered by an external capacitor C_{AVDD} to AVSS.
7	LGPIO6	Dig. I/O	3.3 V general purpose pins to be used as digital I/O or analog input. Input: floating, weak pull-up/pull-down, or single-ended analog input. Output: push-pull or open drain. LGPIO5 and LGPIO6 can be used for differential sensing of positive input voltages, for example to measure the voltage across an external shunt. If not used in the application the pins can be left open. To avoid cross-currents it is recommended to activate the internal pull-down resistors for unused LGPIO pins or alternatively connect unused LGPIO pins to GND.
8	LGPIO5		
9	LGPIO4		
10	LGPIO3		
11	LGPIO2		
12	LGPIO1		
13	LGPIO0		
14	LIN_O	HV I/O	LIN output for LIN auto-addressing in combination with LIN. If not used, LIN_O must be connected to LIN.
15	LIN	HV I/O	LIN transceiver I/O. Alternatively open-drain I/O with pull-up to V_{BAT} programmable by software.
16	BVSS	G	System ground. Internally connected to AVSS with anti-parallel diodes. Connect to AVSS on PCB.
17	TEST	G	Test Input. Must be connected to GND in the application to prevent the IC from entering test mode.
18	MVDD1	HV S	DC-link voltage for the motor and power supply pin of internal half-bridges. Must be connected to BVDD and MVDD0. Requires C_{MVDD} capacitance to BVSS depending on application and motor use.
19	WAKE	HV In	V_{BAT} level pin to wake the device from sleep or monitor supply level voltages.

Table 2–1: Pin List**, continued**

No.	Name	Type[1)]	Module / Function
20	MOUT2	HV Out	Half-bridge for motor control.
21	MVSS1	HV G	Common source of half-bridges. MVSS0 and MVSS1 are internally connected and must be externally connected as well. If external shunt is used, R_{SHUNT} should be placed between MVSS0/1 and GND.
22	MVSS0	HV G	
23	MOUT1	HV Out	Half-bridge for motor control.
24	MOUT0	HV Out	Half-bridge for motor control.
–	Exposed Pad	G	The exposed pad is directly connected to the substrate at the die backside. It is recommended to connect the exposed pad to GND.

[1)]Pin types are defined as:
HV = High voltage
Dig. = Digital voltage
S = IC supply
P = Power supply
G = GND
In = Input
Out = Output
I/O = Input and output

2.3. Package Marking

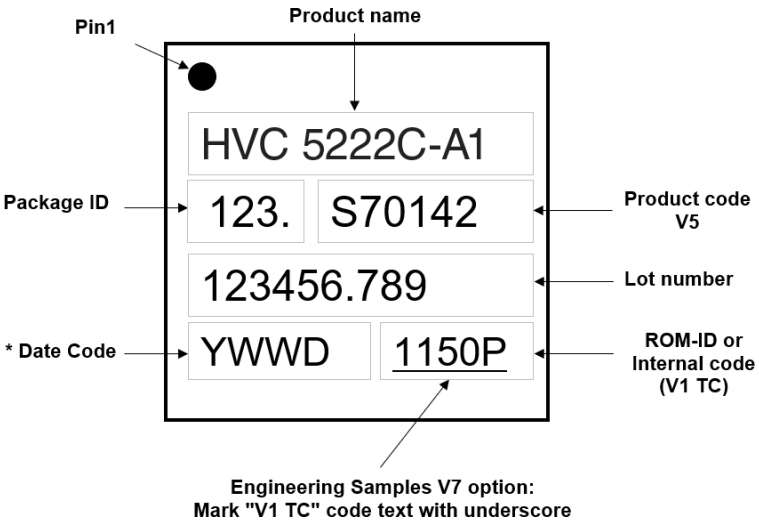


Fig. 2–2: Package marking example of the HVC 5222C in PQFN24 package (text may vary)

2.4. Typical Application Diagrams

The following diagrams show application circuits with suggested components for EMI compatibility and automotive robustness. A bill of materials follows on page 11.

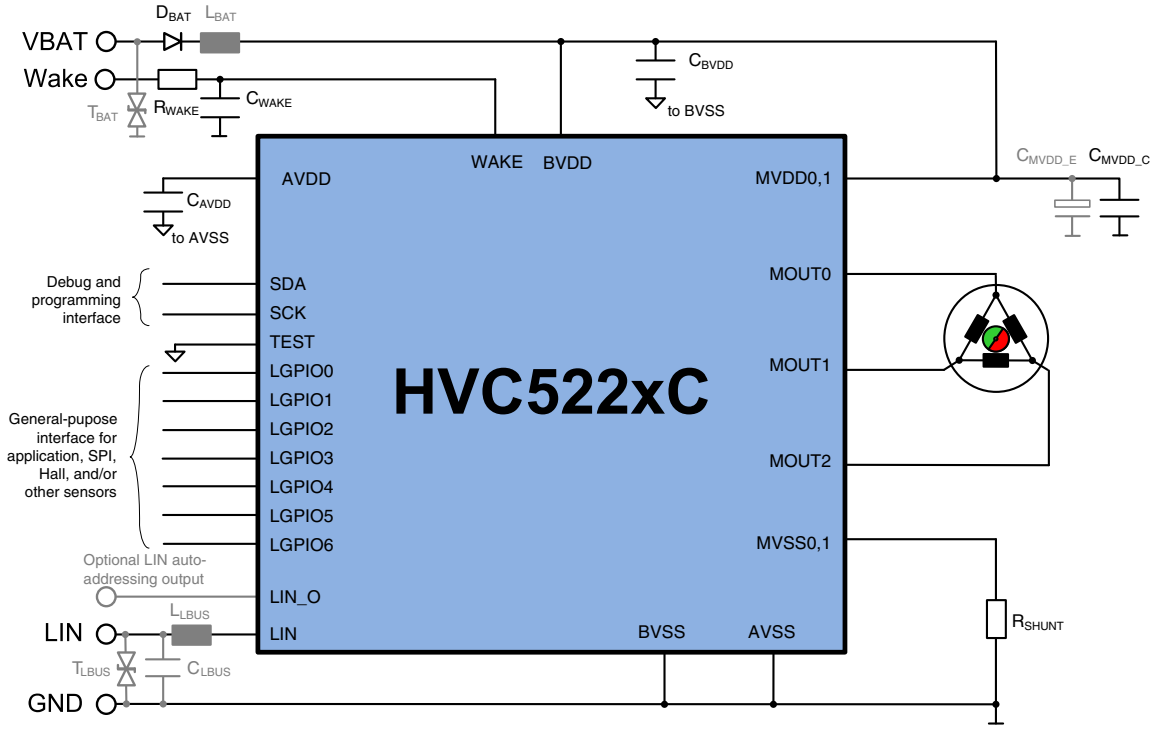


Fig. 2–3: Application circuit for BLDC motor control using wake through Key/KL15

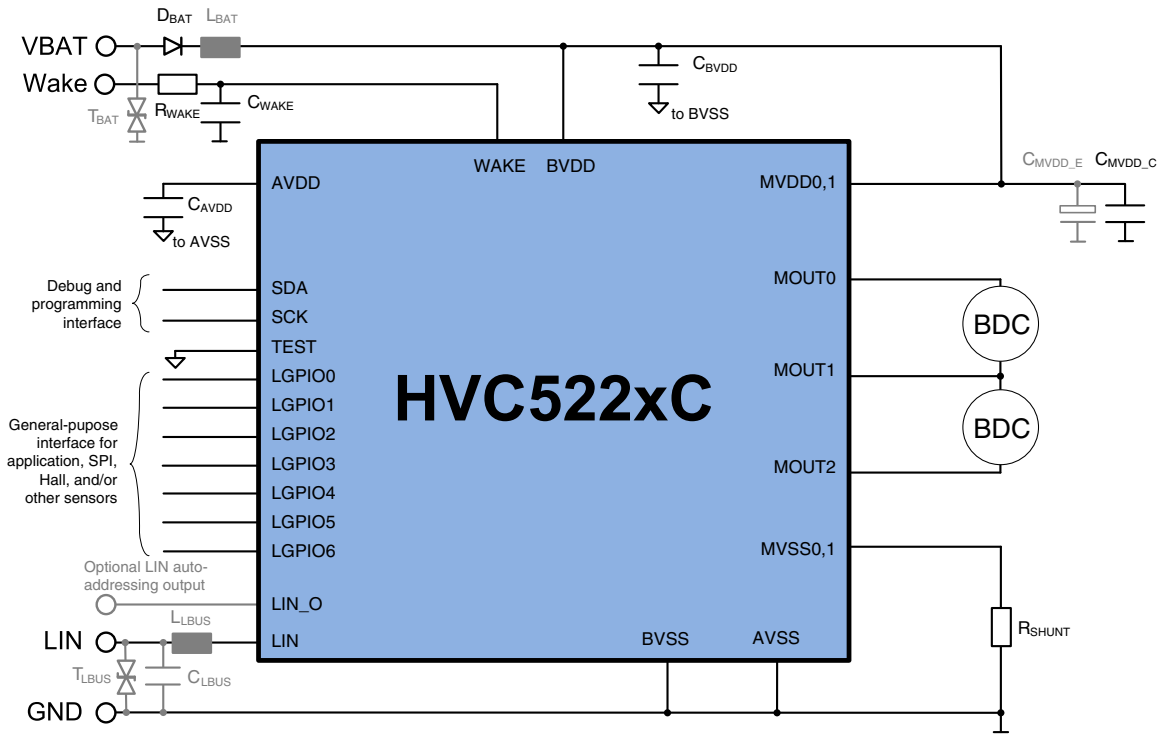


Fig. 2–4: Application circuit for one or two BDC motors.

2.4.1. Bill of Materials (BOM)

Table 2–2: Typical Application BOM Recommendations

Component	Description	Ratings	Recommendation
T_{BAT}	Optional TVS diode to clamp supply.	35 V(max)	SM4T35
D_{BAT}	Reverse polarity diode or P-MOS transistor.	50V, $I_{MOUTpeak_ROC}$*	See Section 2.4.2.1. below.
L_{BAT}	Optional ferrite to improve EMC.	$I_{MOUTpeak_ROC}$*	
C_{MVDD_C}	Ceramic DC-Link capacitance.	1 µF(min), 40 V	See Section 2.4.2. below.
C_{MVDD_E}	Optional low ESR electrolytic DC-Link capacitance.		
C_{BVDD}	BVDD capacitor for EMC robustness. Place close to IC.	100 nF, 40 V	ceramic
C_{AVDD}	AVDD capacitor. Place close to IC.	100 nF, 6.3 V	ceramic
T_{LBUS}	Optional TVS diode to clamp LIN bus.	27 V	MMBZ27VCL
L_{LBUS}	Optional ferrite to improve LIN EMC.	100 mA	BK1005HW601-TV
C_{LBUS}	Optional capacitor to improve LIN EMC.	220 pF, 40 V	ceramic
R_{SHUNT}	HVC 5222C external current measurement resistor.	300 mΩ, 1/2 W	2 %
R_{WAKE}	Input protection resistor for external WAKE.	10 kΩ, 1/8 W	
C_{WAKE}	Input protection capacitor for external WAKE.	100 nF, 40 V	

* Depending on version, see “Recommended Operating Conditions” on page 17

2.4.2. Design and Layout Considerations

A two-layer PCB is required for optimal thermal performance of the HVC 5222C package. The exposed pad of the IC must be connected to the backside of the PCB using thermal vias. It is recommended to implement a GND plane at the back of the PCB. The following current paths need to be dimensioned to carry maximum motor current:

– VBAT terminal to MVDD0/1
  MVDD0/1 must be connected on the PCB with a low-impedance connection.
– MOUTx to motor terminals
– MVSS0/1 to GND terminal
  Can be connected to the exposed pad under the IC unless an external shunt is used.

The DC-Link capacitance C_{MVDD} between MVDD0/1 and GND serves as a high-frequency buffer for the motor currents and should be as close to the IC as possible. It has the following purpose:

– Buffer high-frequency motor currents.
– Store BEMF energy during back-drive and braking conditions.
– Store free-wheeling energy.
– Extend operation time of the HVC 5222C during undervoltage transients for controlled shut-down.

Using all ceramic capacitors is ideal for performance, but a combination of electrolytic and ceramic is possible. In that case at least a 1 µF ceramic capacitor must be used and care must be taken to account for the thermal performance of electrolytic capacitors.

BVSS and AVSS can be directly connected to the exposed pad. The AVDD blocking capacitor C_{AVDD} should be placed right across the pins AVDD and AVSS. The HF bypass capacitor C_{BVDD} should be connected to BVDD directly and to the GND plane of the PCB using as many vias as possible.

LIN HF and protection circuitry should be close to the LIN connector. Added inductance to the pins helps with EMI performance. An optional external LIN bus shunt between LIN and LIN_O must be positioned close to the pins.

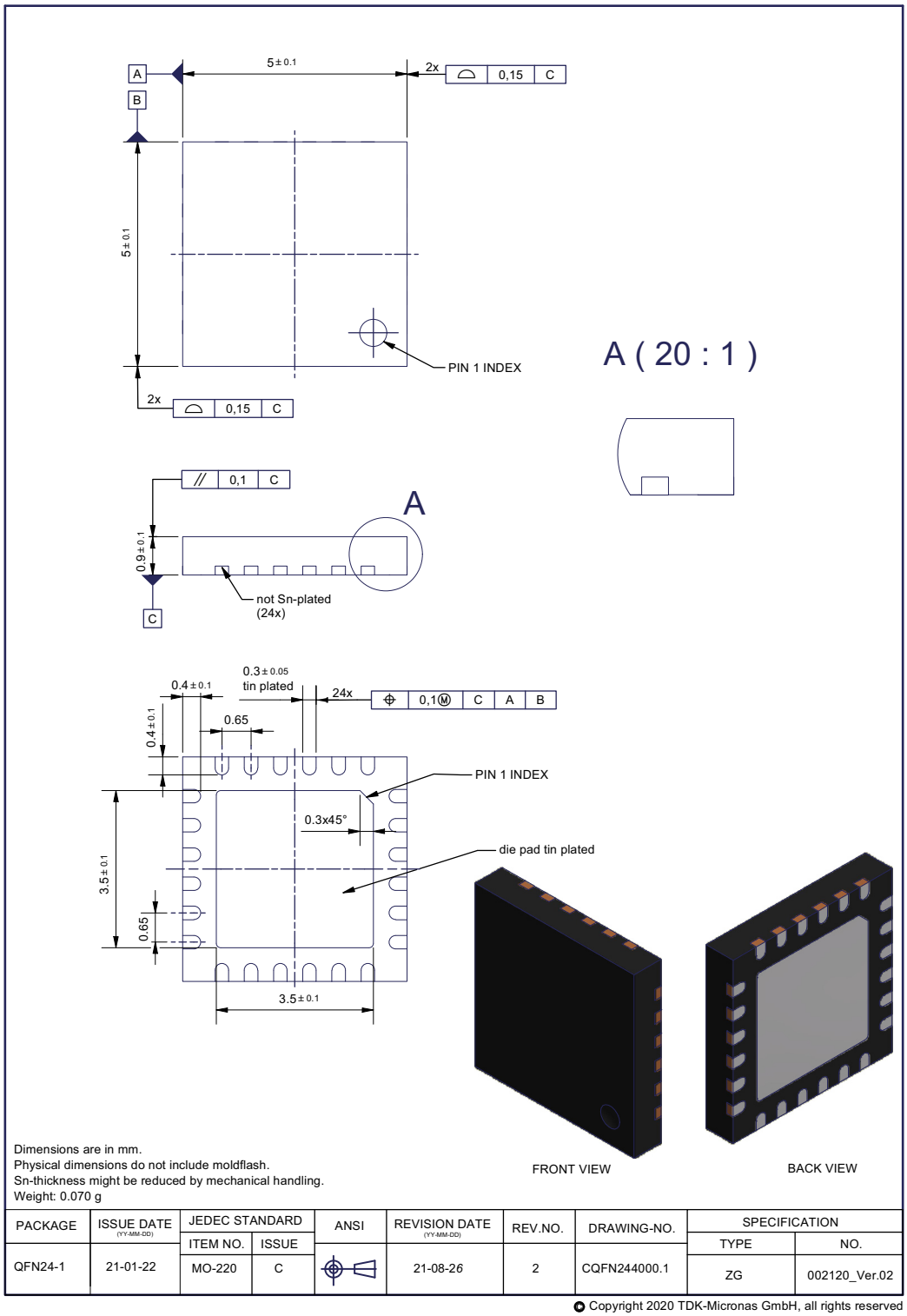
2.4.2.1. Reverse-Polarity Protection

The HVC 5222C must be protected against reverse polarity using a diode or a MOSFET. If the motor does not typically operate in generator operation, a diode is recommended, as it insulates the application better from transient disturbances and extends IC operating time during undervoltage events.

If the motor is used in generator mode (active braking, recuperation) the following options are available:

– A reverse-polarity diode D_{BAT} can be used if
  - The DC-link capacitance C_{MVDD} is large enough to store the recuperation energy and prevent the supply voltage from rising above $V_{SUPBAMR}$(max = 40 V).
  - A clamp circuit (TVS or active clamping) is included in the application to keep the DC Link voltage $V_{MVDD0,1}$ below $V_{SUPBAMR}$.
– A P-MOS switch is placed in the reverse-polarity path to allow for returning the energy to the vehicle supply. The P-MOS circuit must be designed to turn off in case of reverse-polarity.

2.5. Package Outline Dimensions



Dimensions are in mm.
Physical dimensions do not include moldflash.
Sn-thickness might be reduced by mechanical handling.
Weight: 0.070 g

PACKAGE	ISSUE DATE (YY-MM-DD)	JEDEC STANDARD		ANSI	REVISION DATE (YY-MM-DD)	REV.NO.	DRAWING-NO.	SPECIFICATION	
		ITEM NO.	ISSUE					TYPE	NO.
QFN24-1	21-01-22	MO-220	C		21-08-26	2	CQFN244000.1	ZG	002120_Ver.02

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Fig. 2–5:
PQFN24-1: Plastic **Q**uad **F**lat **N**on-leaded package, **24** pins, 5 × 5 × 0.85 mm^3, 0.65 mm pitch

3. Electrical Data

Note All voltages listed are referenced to V_{BVSS} = V_{AVSS}= 0 V and V_{BVDD} = V_{MVDD0} = V_{MVDD1}. Ground pins BVSS, AVSS, and the exposed pad must be connected to a low-resistive ground plane close to the IC. Negative currents indicate currents flowing out of the chip. All parameters are valid for the supply voltage range 6 V < V_{BVDD} < 18 V from T_J = –40 °C to 150 °C for all variants of the HVC 5222C unless otherwise noted.

3.1. Absolute Maximum Ratings

This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum ratings conditions for extended periods will affect device reliability. Stress conditions beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

Table 3–1: Absolute Maximum Ratings

Parameter	Pin	Symbol	Min.	Max.	Unit	Conditions
Supply Voltage						
Main supply voltage	BVDD MVDD0 MVDD1	$V_{SUPBAMR}$	–0.3	40	V	
Main supply voltage slope	BVDD, MVDD0 MVDD1	$DV/Dt_{VSUPBAMR}$		10	V/µs	V_{BVDD} < 19 V. For 19 V < V_{BVDD} < 40 V refer to max. main V_{SUP} slope value according to ISO 16750-2:2012 (former pulse 5b).
Motor bridge ground	MVSS0 MVSS1	$V_{MVSSAMR}$	–0.3	0.3	V	
Supply Currents						
Supply current BVDD	BVDD BVSS	$I_{SUPBVDDAMR}$	–100	100	mA	Supply current limitation with respect to product reliability over lifetime (e.g. due to electro-migration). The current can be interpreted as an RMS value.
Motor supply current HVC 5222C	MVDD0 MVDD1 MVSS0 MVSS1 MOUTx	$I_{SUPMotAMR}$	–1500	1500	mA	With MOUTx limits for I_{outRMS} and $I_{outpeak}$ according to the recommended operating conditions.
Digital Output Current						
Output current LGPIOx pins and SDA pin	LGPIOx SDA	I_{outAMR}	–15	15	mA	
Sum of output currents from AVDD regulator for LGPIO pins and from AVDD pin	LGPIOx SDA AVDD	$I_{outTotalAMR}$	–30		mA	

Table 3–1: Absolute Maximum Ratings

Parameter	Pin	Symbol	Min.	Max.	Unit	Conditions
Input Voltage						
Input voltage MOUT pins	MOUTx	$V_{inMOUTAMR}$		40	V	5 × 400 ms, with 30 sec. period.1 h cumul. max. The application SW has to take measures to reduce the motor-current or to turn off the motor in overvoltage mode. It is recommended to stop the motor and to turn on all power-bridge low-side MOSFETs. Dynamically lower voltages during free-wheeling are covered by the maximum specified phase currents.
Input voltage LGPIOs	LGPIOx SDA SCK TEST	$V_{in3V3AMR}$	1		V_{AVSS} –0.3 V	
Input voltage LGPIOs	LGPIOx SDA SCK TEST	$V_{in3V3AMR}$		1	V_{AVDD} +0.3 V	
Input voltage LIN pin	LIN	$V_{inLINAMR}$	–27	40	V	
Thermal Ratings						
Junction temperature under bias		T_{JAMR}	–40	175	°C	The thermal shutdown (TSD) is generated between +165 °C < T_J < +175 °C, forcing the device into reset state.
Transportation/Short Term Storage Temperature		T_{SAMR}	–55	150	°C	Device only without packing material.

3.2. ESD and Latch-Up

This device contains circuitry to protect the inputs and outputs against damage due to high electrostatic voltages or electrical fields as specified. It is advised that precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages (see “Absolute Maximum Ratings” on page 14).

Table 3–2: ESD and latch-up

Parameter	Pin	Symbol	Min.	Max.	Unit
Maximum latch-up free current HVC 5222C (according to AEC-Q100-004 Grade 1 at T_A = +125 °C)	MOUTx	$I_{latchMOUT}$	–1500	1500	mA
	all other	I_{latch}	–100	100	mA
Human body model, equivalent to discharge 100 pF with 1.5 kΩ (measurement according to AEC-Q100-002)	LIN[1)]	V_{HBM_LIN}	–8	8	kV
	all other	V_{HBM}	–2	2	kV
Human body model, equivalent to discharge 100 pF with 1.5 kΩ (measurement according to AEC-Q100-002)	BVDD MVDD0 MVDD1	$V_{HBMxVDD}$	–4	4	kV
According to IEC 61000-4-2 (330 Ω 150 pF)	LIN[1)]	$V_{SystemESD}$	–6	6	kV
Charged device model (measurement according to AEC-Q100-011)	All	V_{CDM}	–750	750	V

[1)] According to OEM requirement specification “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications v1.3” from May 4, 2012. Further components like varistor, TVS diode or passives might be necessary to fulfill requirements of other OEM specifications.

3.3. Transient Supply Voltages

Automotive test pulses are applied on module level according to ISO7637 at room temperature and a typical battery voltage of 13.5 V. The IC pins used to connect the module to the wiring harness shall be used with the protection circuitry described in the conditions. See also application circuits in Section 2.4..

Table 3–3: Transient supply voltages

Parameter	Min.	Max.	Unit	Condition
ISO 7637-2:2011 pulse 1	–100		V	External reverse polarity diode.
ISO 7637-2:2011 pulse 2a		+75	V	External reverse polarity diode and TVS diode. 1 µF blocking capacitor C_{BVDD} with low ESR.
ISO 7637-2:2011 pulse 2b		+10	V	
ISO 7637-2:2011 pulse 3a	–150		V	With reverse polarity diode.
ISO 7637-2:2011 pulse 3b		+100	V	External TVS Diode.
ISO 16750-2:2012	3.2		V	Values according to OEM specifications.
ISO 16750-2:2012		+40	V	< 400 ms duration.
ISO 16750-2:2012		+28	V	< 2 min duration.

3.4. Recommended Operating Conditions

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. Failure to comply with the above recommendations will result in unpredictable behavior of the device and may result in device destruction. Functional operation of the device at conditions beyond those indicated in the “Recommended Operating Conditions” is not implied and may result in unpredictable behavior, reduce reliability and lifetime of the device.

External components and connections according to “Typical Application Diagrams” on page 10. All externally applied discrete components must be selected according to the required temperature range in the application.

Table 3–4: Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltages (BVDD, MVDD, MVSS)						
Main supply voltage	V_{SUPB_ROC}	6	14	18	V	
Main supply voltage	$V_{SUPBEXT_ROC}$	4.8		40	V	1)2)3) Load-dump: 5 × 400 ms, with 30 sec. period. Cumulative 1 h max. Refer to Table 3–3 for transient supply voltages.
Main supply voltage during RETENTION mode	$V_{SUPBRETENTION_ROC}$	2.5			V	RAM content is preserved. No CPU function. Return from RETENTION mode with POR.
Motor bridge ground	V_{MVSS_ROC}	–0.065		0.3	V	Minimum value limited due to linearity of ADC. If negative voltage ADC measurement is not needed this voltage can be extended to –0.3 V.
Digital Pins (LGPIOx, SDA, SCK, TEST)						
Input high voltage	V_{ih3V3_ROC}	0.72		1	VAVDD	
Input low voltage	V_{il3V3_ROC}			0.28	VAVDD	
Output current	$I_{LGPIOout_ROC}$	–4		4	mA	
MOUT Pins (MOUTx)						
RMS output current HVC 5222C	$I_{MOUTRMS_ROC}$	–600		600	mA	
MOUTx Peak output current HVC 5222C	$I_{MOUTpeak_ROC}$	–1000		1000	mA	t_{ON}<1 s (single MOUT)
LIN Transceiver (LIN, LIN_O)[3)]						
LIN bus voltage	V_{BUS_ROC}	–2.7		20.7	V	Reduced functionality for LIN bus voltage > $V_{BUS_ROC(max)}$
AVDD Regulator, 3.3 V supply voltage (AVDD)						
Output current	$I_{AVDDout_ROC}$	–15			mA	with C_{AVDD} = 100 nF
External AVDD buffer capacitor	C_{AVDD_ROC}	80	100	120	nF	Capacitor has to be selected according to the required temperature range in the application.

Table 3–4: Recommended Operating Conditions**, continued**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Temperature Conditions						
Thermal resistance from junction to ambient	R_{thJA}			30	K/W	Parameter is simulated with model of 2-layer JEDEC board (1s1p) with thermal vias. Values are only valid if the exposed pad is soldered onto the PCB.
Thermal resistance from junction to case	R_{thJC}			13	K/W	
Junction temperature under bias	T_{J_ROC}	–40		150	°C	The thermal shutdown (TSD) is generated between +165 °C < T_J < +175 °C, forcing the device into reset state (see Section 4.6.)
Ambient temperature under bias	T_{A_ROC}	–40		125	°C	AEC-Q100 Temperature Grade 1

1) Some analog parameters may degrade and full motor operation is not guaranteed.

2) If V_{BVDD} > 18 V the application software is responsible to limit the power dissipation to keep T_J inside Recommended Operating Conditions.

3) Compliant with LIN Physical Layer Specification described in ISO 17987-4 / SAE J2602.

3.5. Electrical Characteristics

Table 3–5: Electrical Characteristics

Parameter	Symbol	Min.	Typ.[1)]	Max.	Unit	Conditions
System Supplies (BVDD, MVDD0,1)						
Supply OVERVOLTAGE threshold	V_{BVDDO}	28	29		V	Operation above 18V degrades lifetime performance. See ROC Section 3.4.
Supply UNDERVOLTAGE threshold	V_{BVDDU}	5.3		5.9	V	optionally LIN recessive
POR to ACTIVE for V_{BVDD} rising	V_{RET}			4.6	V	
ACTIVE to RETENTION for V_{BVDD} falling	V_{POR}			4.8	V	2)
RETENTION to POR for V_{BVDD} falling	$V_{PORretention}$			2.5	V	2)
SLEEP to POR asserted for V_{BVDD} falling	$V_{PORsleep}$	1.5	2.5		V	2)
Thermal shutdown to POR asserted for V_{BVDD} falling				1.5	V	2
Active mode supply current HVC 5222C	I_{DDP}	10	14	18	mA	f_{SYS}= f_{CPU}= 20 MHz V_{BVDD}= 12 V
Sleep mode supply current	I_{DDSL}		35	50	µA	2)3) T_A = T_J < 105 °C V_{BVDD} < 13.5 V, LIN = recessive
				100	µA	2)3) as above, V_{BUS} = 0 V
				100	µA	2)3) T_A = T_J < 150 °C V_{BVDD} < 13.5 V, LIN = recessive
Power-up time	t_{PU}			2	ms	Guaranteed by design Defines the time from V_{BVDD} permanently exceeding V_{POR} until the first code execution from flash memory.
Wake-up time trough WAKE or LIN wake pulse.	t_{WU}			2	ms	3) Guaranteed by design V_{BVDD} = 13.5 V. Defines the time from valid WAKE or LIN wake until execution of the first code in the flash memory.
Linear Regulator (AVDD)						
Analog Supply Voltage	V_{AVDD}	3.2	3.3	3.4	V	-15 mA continuous, -30 mA peak
Overvoltage RESET Threshold	V_{AVDDOV}	3.8			V	2) CPU in RESET state
Undervoltage RESET Threshold	V_{AVDDUV}			3.2	V	

Table 3–5: Electrical Characteristics**, continued**

Parameter	Symbol	Min.	Typ.[1)]	Max.	Unit	Conditions
Digital Pins (LGPIOx, SDA, SCK, TEST)						
Input low-to-high threshold	V_{ilh3V3}			0.72	V_{AVDD}	
Input high-to-low threshold	V_{ihl3V3}	0.28			V_{AVDD}	
Input schmitt trigger hysteresis	$V_{hyst3V3}$	0.5			V	[2)]
Input high current	$I_{ihigh3V3}$	–5		5	µA	V_{in}= V_{AVDD}. No internal weak pull-up/down configuration applied.
Input low current	$I_{ilow3V3}$	–5		5	µA	V_{in}= 0 V
Output high voltage	V_{oh3V3}	0.8			V_{AVDD}	I_{oh}= 4 mA
Output low voltage	V_{ol3V3}			0.4	V	I_{ol}= –4 mA
Weak pull-down resistor	R_{pd}	80		210	kΩ	V_{in}= V_{AVDD}. LGPIO internal weak pull-down configuration applied.
Weak pull-up resistor	R_{pu}	80		210	kΩ	V_{in}= 0 V. LGPIO internal weak pull-up configuration applied.
MOUT Pins (MOUT0,1,2)						
Static drain-source on-resistance of high-side N-MOS HVC 5222C	$R_{DS(ON)hs}$		0.9	1.3	Ω	I_{MOUT}= –100 mA
Static drain-source on-resistance of low-side N-MOS HVC 5222C	$R_{DS(ON)ls}$		0.9	1.3	Ω	I_{MOUT}= 100 mA
Overcurrent shutdown in high-state HVC 5222C	Iocshi	–2.0		–1.1	A	With HS OC enabled
Overcurrent shutdown current in low-state HVC 5222C	Iocslo	1.1		1.5	A	
MOUT pull-down resistor network (BEMFC reference voltage)	R_{MOUT}	72	96	120	kΩ	V_{MOUT0} = V_{MOUT1}= V_{MOUT2}
BEMF comparator delay time	BEMFC delay		500	550	ns	[3)]
BEMF comparator hysteresis	BEMFChyst	30		70	mV	[2)] Measured with 40 kHz input ramp signal
WAKE Pin						
Wake threshold WAKE rising	V_{ihWAKE}	3.0		4.5	V	
WAKE pull-down resistor network	R_{MOUT}	72	96	120	kΩ	

Table 3–5: Electrical Characteristics**, continued**

Parameter	Symbol	Min.	Typ.[1)]	Max.	Unit	Conditions
12-Bit A/D Converter						
ADC differential non-linearity including the signal path: difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included.	$DNL_{ADC\&SP}$	–4		4	LSB	2)
ADC integral non-linearity including the signal path: difference between the output of an actual ADC and the line best fitting the output function (best-fit line)	$INL_{ADC\&SP}$	–8		8	LSB	2)
LSB value of the ADC	$LSB_{ADC\&SP}$		1.61		mV	Guaranteed by design
ADC signal-path warm-up time	t_W			10	µs	2)
Conversion time	t_c		1		µs	Excluding f_{MAIN} tolerance.
ADC linear input voltage range BVDD vs. AVSS	$V_{inAdcBVDD}$	6		18	V	2) GPGA = 1
Signal Path Error BVDD	SPE_{BVDD}	–2		2	%	
ADC Zero error	$ZE_{AdcBVDD}$	–10		10	LSB	
ADC linear input voltage range LGPIO vs. AVSS	$V_{inAdcLGPIO}$	0		3.3	V	2) GPGA = 1
Signal Path Error LGPIO	SPE_{LGPIO}	–3		3	%	
ADC Zero error	$ZE_{AdcLGPIO}$	–10		10	LSB	
ADC linear input voltage range LGPIO5 vs. LGPIO6	$V_{inAdcLGPIO-diff}$	–3.3		3.3	V	2) GPGA = 1
Signal Path Error LGPIO5/6	$SPE_{LGPIOdiff}$	–3		3	%	
ADC Zero error	$ZE_{AdcLGPIO-diff}$	–10		10	LSB	
ADC linear input voltage range MOUTx phase voltage	$V_{inAdcMOUT}$	0		9.9	V	2) GPGA = 4
Signal Path Error MOUTx	SPE_{MOUT}	–4		4	%	
ADC Zero error	$ZE_{AdcMOUT}$	–10		10	LSB	
ADC linear input voltage range WAKE pin voltage	$V_{inAdcMOUT}$	0		9.9	V	2) GPGA = 4
Signal Path Error MOUTx	SPE_{MOUT}	–4		4	%	
ADC Zero error	$ZE_{AdcMOUT}$	–10		10	LSB	
ADC linear input voltage range external shunt MVSSx vs. BVSS	$V_{inAdcMVSSx}$	–0.065		0.3	V	2) GPGA = 8
Signal Path error MVSSx	SPE_{MVSSx}	–4		4	%	
ADC Zero error	$ZE_{AdcMVSSx}$	–10		10	LSB	

Table 3–5: Electrical Characteristics**, continued**

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Conditions
Temperature Sensor and Supervision						
Temperature error of temperature sensor read out by ADC	ΔT	–10		10	°C	[2]
Thermal shutdown temperature	T_{TSD}	165	170	175	°C	[2]
Thermal shutdown return temperature	T_{TSDR}	125	140	155	°C	[2]
Oscillators						
Auxiliary oscillator frequency	f_{AUX}	21	35	49	kHz	
Main oscillator frequency	f_{MAIN}	38	40	41	MHz	With ERM off
Embedded Flash Memory includes EEPROM and NVR						
Flash memory endurance write/ erase cycles	N_{Fwe}	20000			cycles	Qualified according to AEC-Q100 for temp. Grade 1.
Flash sector erase time	t_{FERASE}			12.5	ms	Sector erase
Flash full erase time	$t_{FFERASE}$			30	ms	Full erase
Time to store single Flash word	t_{FPROG}			70	µs	Storage time for single Flash word
Flash memory data retention	t_{Fret}	15			years	According to mission profile. Qualified according to AEC-Q100 for Temperature Grade 1.

[1] Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied, and are not 100% tested.
[2] Parameter is derived from design characterization on a small sample size
[3])Compliant with LIN Physical Layer Specification described in ISO 17987-4

3.5.1. LIN Transceiver Characteristics

The LIN transceiver is compliant to ISO17987 physical layer conformance specification. LIN_CR.LOM must be set to '0' (reset value) to be LIN compliant..

Table 3–6: Characteristics – LIN Transceiver

Parameter	Symbol	Min.	Typ.[1)]	Max.	Unit	Conditions
LIN capacitance	C_{LIN}	30	48	60	pF	Guaranteed by design with respect to ISO17987 physical layer conformance test specification
Falling edge slew rate	DV/Dt_{fall}		1.5		V/µs	[2)] SR = 2
Falling edge slew rate	DV/Dt_{fall}		10		V/µs	[2)] SR = 0, with bus-load C_{BUS} = 1 nF and R_{BUS} = 1 kΩ.
Maximum rising edge slew rate (depending on external pull-up resistor)	$DV/Dt_{risemax}$		1.5		V/µs	[2)] SR =2
Maximum rising edge slew rate (depending on external pull-up resistor)	$DV/Dt_{risemax}$		10		V/µs	[2)] SR = 0, with bus-load C_{BUS} = 1 nF and R_{BUS} = 1 kΩ.
Receiver propagation delay	trxpd			6	µs	
Receiver propagation delay symmetry	trxsym	–2		2	µs	
Low pulse time for wake-up. A LIN wake-up occurs with a low-pulse on the LIN-bus with the length t_{WUP}. The dominant to recessive bus transition of this pulse wakes the LIN device.	twup	28		150	µs	$V_{BUS} < V_{BVDD}$ / 2 - 360 mV. Min. value from "HW Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications v1.3 / May 4th,2012". Max. value from "LIN Spec."
Current shutdown threshold for driver dominant state	I_{BUS_LIM}	40		200	mA	V_{BUS}= 18 V, driver on
Leakage current at BVDD loss	$I_{BUS_NO_BAT}$			30	µA	V_{BVDD}=V_{GND}, 0V < V_{BUS} < 18 V, V_{BAT} disconnected
Leakage current at ground loss	$I_{BUS_NO_GND}$	–1		1	mA	V_{GND} = V_{BVDD}, 0 V < V_{BUS} < 18 V, V_{BAT} = 12 V
Input leakage current at the receiver inclusive pull-up resistor as specified	$I_{BUS_PAS_dom}$	–1			mA	V_{BUS} = 0 V, V_{BAT} =12 V, driver off
Leakage current at the receiver inclusive pull-up resistor as specified	$I_{BUS_PAS_rec}$			20	µA	8V < V_{BUS} < 18 V, 8 V < V_{BAT} < 18 V, V_{BUS} >= V_{BAT}, driver off
LIN slave internal pull-up resistance at output	R_{SLAVE}	20	30	60	kΩ	
Center of receiver threshold	V_{BUSCNT}	0.475	0.5	0.525	V_{BVDD}	V_{BUS_CNT} = (Vth_dom + Vth_rec)/2
Transmitter recessive voltage	V_{BUSOH}	0.8		1	V_{BVDD}	

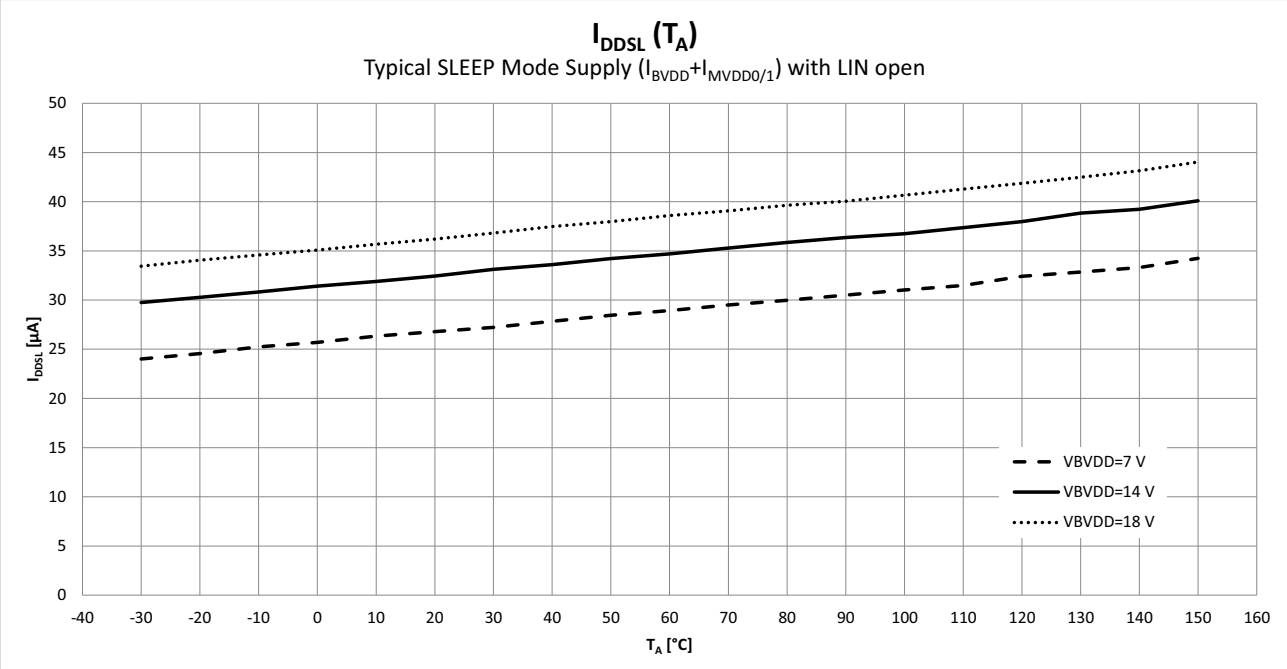
Table 3–6: Characteristics – LIN Transceiver

Parameter	Symbol	Min.	Typ.[1)]	Max.	Unit	Conditions
Transmitter dominant voltage	V_{BUSOL}			0.2	V_{BVDD}	R_{BUS} = 500 Ω
Receiver dominant state	V_{BUSdom}			0.4	V_{BVDD}	Without external diode
Receiver recessive state	V_{BUSrec}	0.6			V_{BVDD}	Without external diode
Hysteresis of receiver threshold	V_{HYS}			0.175	V_{BVDD}	V_{HYS} = Vth_rec - Vth_dom
Driver (LIN driver bus load conditions (C_{BUS}, R_{BUS}) according to ISO17987)						
LIN Duty Cycle 1	D1	0.396			BVDD	TH_REC(max)= 0.744 × V_{BVDD}, TH_DOM(max)= 0.581 × V_{BVDD}, V_{BVDD}= 7.0 V to 18 V, D1= t_busrec(min)/(2 × t_bit)
LIN Duty Cycle 2	D2			0.581	BVDD	TH_REC(min)= 0.422 × V_{BVDD}, TH_DOM(min)= 0.248 × V_{BVDD}, V_{BVDD}=7.6 V to 18V, D2= t_busrec(max)/(2 × t_bit)
LIN Duty Cycle 3	D3	0.417			BVDD	TH_REC(max)= 0.778 × V_{BVDD}, TH_DOM(max)=0.616 × V_{BVDD}, V_BVDD=7.0 V to 18 V, D3= t_busrec(min)/(2 × t_bit)
LIN Duty Cycle 4	D4			0.59	BVDD	TH_REC(min)= 0.389 × V_{BVDD}, TH_DOM(min)= 0.251 × V_{BVDD}, V_{BVDD} = 7.6 V to 18 V, D4= t_busrec(max)/(2 × t_bit)
Auto-Addressing (LIN, LIN_O)						
Current source	I_{CS}	1.85	2.05	2.25	mA	
Bus-shunt resistor	R_{BSM}	0.65		1	Ω	

1) Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied, and are not 100% tested.

2) Parameter is derived from design characterization on a small sample size

3.5.2. Typical Operating Conditions



3.5.3. Supply Current vs. Temperature in SLEEP Mode

4. Functional Description

The following section provides an overview of the functions and features implemented in the HVC 5222C. For a detailed description of the device and how to program it see the corresponding user guide.

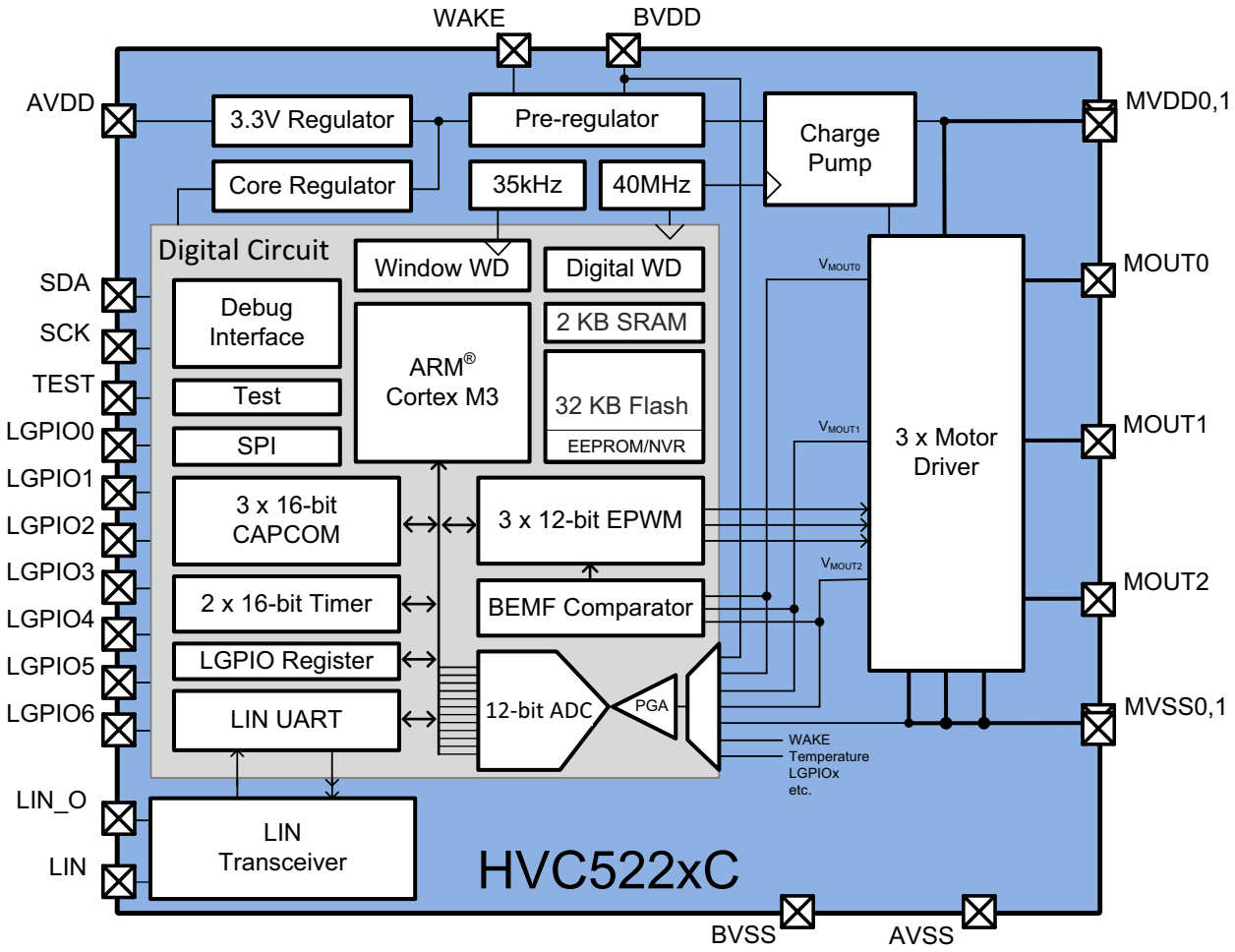


Fig. 4–1: Block diagram of the HVC 5222C

4.1. Power Supplies

The HVC 5222C can be directly connected to the 12 V automobile on-board power supply (KL30) and withstands all disturbances appearing on the car's supply, specified in ISO 7637-2:2004. The reverse polarity protection for the HVC 5222C should be provided by an external device.

A separate voltage regulator for the system supply is not required as the HVC 5222C generates all internal voltages directly from BVDD.

4.1.1. Power-up

After the voltage at BVDD has passed the power-on reset threshold V_{POR} = 4.8 V(max), the HVC 5222C ramps up its internal power supplies and code execution in Flash will start within t_{PU} = 2 ms(max).

4.1.2. Wake-up

The HVC 5222C can be woken from SLEEP mode via a LIN “wake” pulse or a high voltage on WAKE, if so configured by software. This allows application designs such as wake on Key/KL15, wake on button, or wake on motor activation via BEMF voltage. In either case, the wake pulse has to be applied for at least t_{wup}= 150 µs(max) during SLEEP mode. After a wake condition was detected, code execution in Flash will start within t_{WU} = 2 ms(max).

Only the software can put the IC into SLEEP mode.

For external wake-up by KEY/KL15 use see “Application circuit for BLDC motor control using wake through Key/KL15” on page 10.

Note The WAKE wake-up input is disabled at POR and has to be activated by software before entering SLEEP mode. To monitor WAKE outside of SLEEP mode, the corresponding ADC channel has to be sampled by the ADC.

4.1.3. Cold-Crank and Start-Stop Operation

The HVC 5222C includes features to keep the application alive during voltage drops e.g. at car engine start-up (cranking- and start-stop conditions). In this case if the voltage at BVDD drops from its typical value below V_{BVDDU} = 5.9 V(max), an undervoltage interrupt is asserted allowing the software to prepare for undervoltage shutdown.

4.1.3.1. Undervoltage Shut-down and Recovery

The size of the DC-link capacitance C_{MVDD} behind the reverse-polarity diode D_{BAT} defines how long the IC will operate between BVDD dropping under the undervoltage interrupt threshold V_{BVDDU} = 5.3 V(min) and entering RETENTION mode V_{RET} = 4.6 V(max). This time t_{UVSD} can be used to save critical systems parameters into the EEPROM. Assuming the motor is not running, this time can be calculated according to the following formula:

$$t_{UVSD} = C_{MVDD} \cdot (V_{BVDDU} - V_{RET}) / I_{DDP}$$

This calculation yields roughly 580 µs for C_{MVDD} = 10 µF. If more time is required, C_{MVDD} must be increased accordingly.

Note A reverse-polarity diode is required to conserve the DC-link voltage for this operation.

Should V_{BVDD} drop below V_{RET} = 4.6 V(max), the HVC 5222C memory contents are retained while analog and digital functions are stopped (RETENTION mode). In this mode, the digital regulator is functional, the peripherals and the Arm® core are kept in reset state and no program is executed. SRAM contents are conserved.

If the supply voltage V_{BVDD} recovers during RETENTION mode the CPU starts from the reset vector and the RETENTION mode is signaled in the reset source status register.

If V_{BVDD} drops below $V_{PORretention}$ = 2.5 V(max), then a POR signal is generated. In such a case the chip starts up in normal power-up mode without retaining the content of the volatile memories (SRAM).

4.1.4. Overvoltage Operation

An overvoltage condition (e.g. during jump start or load dump) on terminal VBAT must be handled by the application software. An overvoltage (OV) interrupt is asserted once BVDD rises above V_{BVDDO} = 28 V(min). In parallel the internal charge pump is stopped, MOUTx go into high-impedance, and LIN is set to recessive state.

Fig. 4–2 summarizes the various BVDD-dependent operating modes:

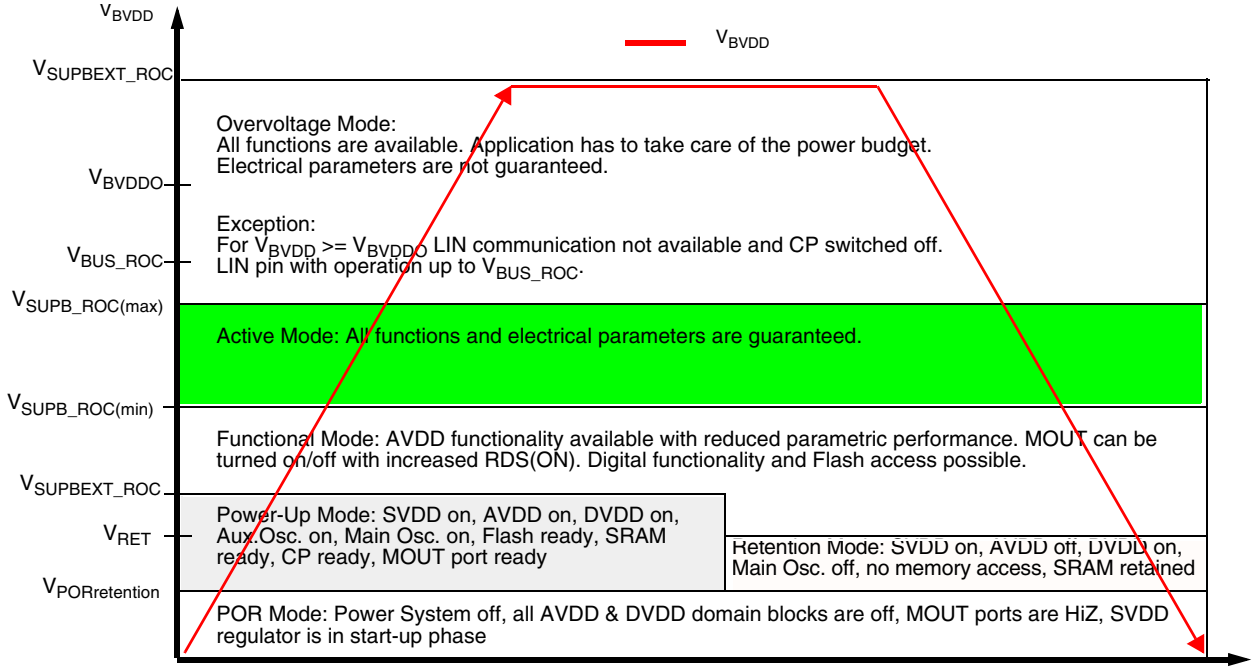


Fig. 4–2: Power mode transitions

4.2. Voltage Regulators

The HVC 5222C features various internal regulators which power the internal digital and analog circuitry:

– The Pre-regulator generates the gate voltages for the internal half-bridges, the secondary supplies and the internal charge-pump.
– A charge-pump boosts the gate voltage above BVDD level.
– A 3.3 V Regulator generates internal analog and digital interface voltage at AVDD.
– A digital regulator generates the internal voltage for the digital block and memories.

The 3.3 V regulator is accessible at AVDD and can be used for supplying external loads. It must be bypassed with an external capacitor C_{AVDD}. External loads must not exceed 15 mA total current, including loads on the LGPIO pins.

4.3. Operating Modes

In order to offer a flexible solution in terms of high system performance and low current consumption, the HVC 5222C provides several operating modes:

– ACTIVE mode, in which all features are available and the CPU is clocked at selectable speed.
– RETENTION mode (2.5 V < V_{BVDD} < 4.6 V), in which the CPU and the peripherals are reset and the RAM content is preserved.
– SLEEP mode (Software activated), in which only few parts of the system are active to achieve low current consumption. Wake-up from SLEEP mode can be triggered either by a low pulse on LIN or a voltage above V_{ihWAKE} = 3.67 V(max) on WAKE if enabled by software.
– OVERVOLTAGE mode (V_{BVDD} > 28 V), in which all features are available but the MOUTx outputs are automatically disabled and the LIN port will be switched to recessive mode. It is recommended to switch off the MOUT port within the BVDD_OV interrupt service routine to prevent damage to the power bridge.
– THERMAL SHUTDOWN mode (T_J > 165 °C(min)), in which the system is reset and only a few modules of the device are active to achieve a minimum of current consumption and to avoid malfunction. It is in the responsibility of the application SW to monitor system junction temperature of the IC and reduce the current consumption of the chip in order to meet the thermal budget of the device and prevent thermal shutdown.

Table 4–1 gives an overview of the operating modes of the internal voltage regulators depending on the chip supply voltage at BVDD.

Table 4–1: BVDD voltage domains

Supply Name	**POR** (0 V<= BVDD < 2.5 V)	**Power-Up** (2.5 V <= BVDD < 4.8 V)	**RETENTION Mode** (2.5 V <= BVDD < 4.6 V)	**ACTIVE Mode*** (4.8 V <= BVDD < 28 V)	**OOVERVOLTAGE Mode** (28 V < BVDD < 40 V)	**SLEEP Mode** (activated by software)	Remarks
SVDD	1	2	2	on	on	on	1 = active, but not functional. V_{SVDD} follows V_{BVDD}. 2 = active, functional above 4.5 V
AVDD	off	off	off	on	on	off	
DVDD	off	off	on	on	on	off	
PVDD	1	1	2	L	L	off	1 = LDO, following V_{BVDD} 2 = BVDD bypass mode L = PVDD Regulator with $V_{PVDD(typ)}$ = 5 V
Charge Pump	off	off	off	on	off	off	
* Regard the quality/reliability restrictions based on recommended operating voltages during ACTIVE mode (see Section 3.4.).							

4.4. Motor Operation

For the control of BLDC or DC motors the HVC 5222C provides the following features:

– Three half-bridges connected to MOUT0,1 and 2. They are supplied by MVDD0/1 and can be connected to ground via MVSS0/1 directly or through an optional external shunt resistor. See also Section 4.4.2.

– The high-side N-channel FETs are driven by gate drivers supplied by an internal charge-pump operating at f_{MAIN} = 40 MHz. To reduce electromagnetic emission energy f_{MAIN} can be modulated by enabling the EMI reduction module (ERM).

– Integrated resistor networks allow ADC measurement of the motor voltages at all MOUTx, as well as BVDD, and BEMF detection for sensor-less BLDC motor control.

– The half-bridges are protected against shoot-through current during switching transitions, overtemperature, and overcurrent and overvoltage. For details, see “Protection Features” on page 35.

Note Both MVDD0/1 and MVSS0/1 are internally connected, so separate operation of the half-bridges on different supplies is not possible.

4.4.1. BLDC Motor Control

For BLDC motor control the three phases of a BLDC motor should be connected to MOUT0, MOUT1, and MOUT2 as illustrated in Fig. 2–3 on page 10.

The voltage levels at the MOUT pins are internally scaled down and connected to the BEMF comparator as well as a multiplexer to be measured via ADC. An internal resistive network is available via multiplexers to generate a virtual starpoint voltage as a reference to detect the BEMF voltage zero-crossing of the floating motor phase.

4.4.2. BDC Motor Control

Two BDC motors can be attached. One between MOUT0 and MOUT1 and a second motor between MOUT1 and MOUT2 (see Fig. 2–4 on page 10).

4.4.3. Analog Measurements

Various internal and external nodes can be measured via the integrated 12-bit ADC. The ADC signal path features a programmable gain amplifier with gain settings x1, x2, x4, x8, and x16.

1. DC Link voltage at BVDD
2. Single-ended input voltage at LGPIO0 to 6
3. Differential input voltage between LGPIO5 and LGPIO6
4. Motor voltages at MOUT0 to 2
5. Voltage at WAKE
6. Voltage at MVSS0/1
7. IC junction temperature
8. LIN Bus-shunt voltage

For more detail also see section “ADC” on page 39.

4.4.3.1. Motor Current Measurement

The motor current flowing through MOUT0, 1 and 2 leaves the IC through MVSS0/1. Attach an external shunt resistor between MVSS0/1 and AVSS to sample the shunt voltage directly at MVSS0/1 through the ADC.

4.4.3.2. Temperature Monitoring

The HVC 5222C features overtemperature detection units to monitor the junction temperature inside the chip for Thermal Shutdown (TSD). They are placed close to the power-bridges, where most of the power in the device is dissipated. If the temperature exceeds T_{TSD} = 165 °C(min) the TSD logic will invoke a TSD reset to protect the device from being thermally destroyed.

An additional linear temperature sensor provides junction temperature information to the application SW via the ADC. By polling the corresponding channel, the application SW can continuously monitor the junction temperature and react on rising temperatures, for example by switching-off modules or reducing the CPU clock.

Note TSD is a device protection mechanism for exceptional failure conditions only. The application SW has to take care that T_J does not exceed 150 °C.

4.5. Application Interface

4.5.1. LGPIO-Ports

Seven LGPIO ports allow implementation of various application functions as well as interfacing to Hall switches or 2D Hall angular sensors for precision motor control. They are implemented as low-voltage general-purpose I/Os. Each LGPIO port can be separately configured to operate in one of several input or output modes:

– input floating

– input analog to be sampled by the internal ADC

– input with weak pull-down

– input with weak pull-up

– output push-pull

– output open drain

In digital input mode the input level of the LGPIO port is signaled in the data input register of the LGPIO module and is also available as input signal for internal digital peripherals (refer to Table 4–3). In analog input mode the input voltage of the according pin is routed to the ADC input multiplexer (see Fig. 4–1) and the corresponding bit in the LGPIO data input register is set to '0'.

All LGPIO pins are configurable in two digital output modes: push-pull or open drain. For each LGPIO pin following two output sources can be selected individually:

– Their output is defined by the contents of the LGPIO data output register.

– Their output is driven by internal digital peripherals.

Table 4–2 shows the functions which can be assigned to the LGPIO Ports.

Table 4–2: LGPIO port function assignments

Pin Name	Port Function LGPIO					Analog Input
	Normal Input	Normal Output	Alternative Output #0	Alternative Output #1	Alternative Input	
LGPIO digital input (floating, pull-up or pull-down), LGPIO digital output (push-pull or open drain), LGPIO analog input						
LGPIO0	LGPIO0.DI	LGPIO0.DO	TIMER0_OUT	TIMER1_OUT	CAPCOM0_IN[1)], TIMER0_IN	ADC0
LGPIO1	LGPIO1.DI	LGPIO1.DO	TIMER1_OUT	CAPCOM0_OUT	CAPCOM1_IN[1)],TIMER1_IN, LINUART_RX	ADC1
LGPIO2	LGPIO2.DI	LGPIO2.DO	LINUART_TX	CAPCOM1_OUT	CAPCOM2_IN[1)], SPI_MISO	ADC2
LGPIO3	LGPIO3.DI	LGPIO3.DO	LINUART_TX	CAPCOM2_OUT	LINUART_RX[1)], SPI_MISO	ADC3
LGPIO4	LGPIO4.DI	LGPIO4.DO	SPI_CSN	TIMER0_OUT	CAPCOM0_IN, TIMER0_IN	ADC4
LGPIO5	LGPIO5.DI	LGPIO5.DO	SPI_SCK	TIMER1_OUT	CAPCOM1_IN, TIMER1_IN	ADC5[2)]
LGPIO6	LGPIO6.DI	LGPIO6.DO	SPI_MOSI	LINUART_TX	CAPCOM2_IN	ADC6[2)]

[1)] With LGPIO_AIS.AISx = 1. Refer to User Guide for more detail.

[2)] Can also operate as differential analog inputs for positive input voltages.

Table 4–3 describes all special function designators used in Table 4–1 and Table 4–3. Refer to the User Guide for the detailed register setup for the alternative function selection.

Table 4–3: Interface Function Designators.

Name	Function
ADCx	Analog input connected to ADC input multiplexer [x:0 to 6]
CAPCOMx_IN	Capture input of the CAPCOM unit channel x [x: 0 to 2]
CAPCOMx_OUT	Compare output of the CAPCOM unit channel x [x: 0 to 2]
LGPIOx_DI	LGPIO port data input register [x: 0 to 6]
LGPIOx_DO	LGPIO port data output register [x: 0 to 6]
LINUART_RX	Receive input line of the LIN UART
LINUART_TX	Transmit output line of the LIN UART (connected to LIN port output multiplexer LMUX)
LIN_DI	LIN port input register (to LIN transceiver receive input)
LIN_DO	LIN port data output (connected to LIN port output multiplexer LMUX)
TIMERx_IN	TIMER module x compare input [x: 0 to 1]
TIMERx_OUT	TIMER module x output [x: 0 to 1]
SPI_SCK	SPI clock
SPI_MOSI	SPI Master Out Slave In
SPI_MISO	SPI Master In Slave Out
SPI_CSN	SPI Chip Select

4.5.2. MOUT Port

The MOUT pins MOUT0 to MOUT2 are intended for direct motor drive. The pins are switched by the integrated power bridges to MVDDx and MVSSx and can be used to drive brushless motors, brushed motors or other loads as described in section “Motor Operation” on page 30. The voltage of each MOUT is fed to an integrated virtual star point comparator and can be sampled by the internal ADC as well.

Each MOUTx pin is also protected against shorts to GND or supply by comparing individual MOUTx currents against low-side FET overcurrent threshold I_{ocslo} and high-side FET overcurrent threshold I_{ocshi}. At phase currents exceeding I_{ocslo} or I_{ocshi}, automatic overcurrent shutoff is implemented and an interrupt is generated. The shutoff is configurable for the affected MOUTx only or all MOUTs in parallel. The affected MOUTx high-side or low-side is signalled in a corresponding overcurrent register.

4.5.3. LIN or PWM Port

The LIN port is mainly used for communication via the LIN bus according to LIN spec ISO 17987-4 / SAEJ 2602-1 for 12 V systems, but can also serve as a high-voltage digital input and open-drain output. An incoming LIN wake pulse or message can be used as wake signal for the system in SLEEP mode.

The following features are included into the LIN Transceiver:

– Overcurrent protection

– Multiple I/O sources selectable (LIN-UART, Timer 0 and 1, LIN_DO)

– Use of LIN for high-voltage PWM input sampling using one of the built-in timers.

– Selectable slew-rates

– Support of LIN tx dominant time-out function to switch off the transmitter if the LIN bus is stuck at dominant level (according OEM requirement specification “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications v1.3” from May 4, 2012)

Table 4–4: LIN port function assignment

Pin Name	Pin Function LIN Port					
	Normal Input	Normal Output	Alternative Output#0	Alternative Output#1	Alternative Output#2	Alternative Input
LIN [1)]	LINUART_RX	LINUART_TX	TIMER0_OUT	TIMER1_OUT	LIN_DO	LIN_DI, TIMER0_IN, TIMER1_IN
LIN_O	For LIN auto-addressing (slave node position detection with BSM) together with LIN pin. Pin is connected internally via shunt resistor R_{BSM}.					

[1)] The LIN can be used as wake-port in the SLEEP mode.

4.5.3.1. High-Voltage PWM input

The LIN port can also be used to sample battery level PWM signals. In this case the LIN input port can be routed towards the internal timers TIMER0 or TIMER1 which can be used to measure frequency and duty cycle of the PWM input signal.

4.5.3.2. LIN Auto-Addressing

In applications where LIN Auto-Addressing is required the HVC 5222C can support by a dedicated IP set. With minimized additional software effort, a LIN slave node address is automatically determined. This helps reducing additional cost for mechanical- or application-related implementations.

– The LIN Auto-Addressing feature is disabled by default.
– To utilize devices with LIN Auto-Addressing enabled, a dedicated license fee has to be agreed with TDK-Micronas.
– Please contact your local sales support for additional information.

4.5.4. Debug and Test Interface

The Pins SDA, SCK, and TEST are physically identical to the LGPIO ports. The SDA pin is implemented as low-voltage digital I/O port with an internal pull-up resistor while the SCK pin is implemented as low-voltage digital input port with an internal pull-down resistor. In normal operating mode the SDA and SCK pins are used to connect an external debugger to the chip. Alternatively the SDA pin can be used as external reset input in application mode. This function has to be activated in a control word within the Flash memory and is only enabled if the debug interface is disabled in parallel.

The TEST pin is used to enter the test mode. In normal application it must be tied to GND.

4.6. Protection Features

The HVC 5222C includes the following protection features which operate outside and above the software layer:

1. Overtemperature shut-down (TSD) at temperatures above T_{TSD} = 165 °C(min).
2. Supply overvoltage interrupt above V_{BVDDO} = 28 V(min) turns off the MOUTs, puts the LIN Transceiver in recessive state, and can trigger an interrupt.
3. Supply undervoltage below V_{BVDDU} = 5.9 V(max) switches the LIN Port recessive depending on setting of the LIN configuration register and generates an optional interrupt.
4. Overcurrent shutoff of MOUTx above I_{ocslo} or below I_{ocshi} can be configured to either switch off all half-bridges or only the affected half-bridge and generate an optional interrupt.
5. Internal cross-current protection against shoot-through current during switching transitions of the MOUT.

4.7. Microcontroller

4.7.1. Core

The HVC 5222C features an Arm® Cortex®-M3 core (revision r2p1) which is an industry-leading 32-bit RISC processor, widespread in the automotive industry. The Arm® Cortex®-M3 is based on a Harvard architecture with a 3-stage pipeline and supports an address space of 4 Gbyte. It executes the Thumb®-2 instruction set for optimal performance and code size, including division and single-cycle multiply, and reaches a high performance of 1.25 DMIPS/MHz at zero wait-states (Dhrystone 2.1).

4.7.1.1. Core Extensions

As the Arm® Cortex®-M3 is targeting a wide range of applications, the processor is based on a modular concept which includes fixed (basic) components (e.g. Arm® core, NVIC) as well as optional core extensions listed below. The configuration for HVC 5222C is as follows:

– NVIC: 19 IRQs, 8 priority levels

– DAP: AHB-AP & SW-DP

– Three data watchpoints

– Flash patch: 8 breakpoint comparators

4.7.1.2. Debug Interface

The Arm® Cortex®-M3 includes a Debug Access Port (DAP), which is used to connect a Debug Port (DP) to the Arm® core to allow external access by a debugger.

For the HVC 5222C the Serial Wire Debug Port (SW-DP) interface is implemented. For the debug interface two dedicated pins, SCK (clock input), and SDA (bidirectional data IO) are reserved. SDA can be programmed as external reset input.

4.7.1.3. Read-Out Protection

By default, the debug interface is disabled. It can be enabled (through the boot-code inside the startup ROM) by a special setting in the exception table inside the Flash or if the Flash is erased.

4.7.2. Clock System

– Factory trimmed +/-5% main oscillator

– Clock pre-scaler

– EMI reduction module

There are two independent on-chip RC oscillators and a clock input for the Arm® debug interface. The main oscillator is combined with an EMI reduction module and provides the operating clock (f_{MAIN} = 40 MHz) to the system. $f_{SYS} = f_{MAIN} / 2$ is directly supplied to the charge-pump and the peripheral modules and, via a configurable pre-scaler (1/N with N = [1, 2...128]) to the Arm® core.

The clock of the auxiliary oscillator (f_{AUX} = 35 kHz) is used to clock the window watchdog for supervising both RC oscillators.

4.7.2.1. EMI Reduction Module

The EMI reduction module (ERM) is capable of reducing electromagnetic radiation that might cause interference to other electronic equipment. By generating a predefined frequency modulation on f_{SYS} the noise emission of the main oscillator is distributed over a defined frequency range, thus reducing the power spectral density of the digital circuit from one single peak at 20 MHz and it's harmonics to a varying spectrum from 18 MHz to 20 MHz.

4.7.3. Reset System

An extensive network of system supervisors feeds into the HVC 5222C reset system to protect against undefined and unintended states. The reset system is divided into two reset domains, one controlled by the system reset (SYS_RES_N) and the other one controlled by the power-on reset (POR_RES_N).

Table 4–5: Reset Sources Overview

Domain	Reset Source	Comment
Power-On Reset POR_RES_N	Supply (BVDD) Monitoring	Power System Ramping up or down, including ISO transients
	AVDD Monitoring	V_{AVDD} excursion caused by supply drops or external loads
	Internal Supply Monitoring	Various internal supply excursions caused by system damage
	Thermal Shutdown (TSD)	Temperature excursion beyond maximum junction temperature
	Sleep Mode	Software induced sleep mode
System Reset SYS_RES_N	Debugger Reset	External debug interface reset
	Watchdog Resets	Clock deviations or software excursions
	Forced Hardware Reset	Software induced system reset
	External SDA Reset	Active-low digital signal at SDA after SDA reset was enabled

During a power-on reset, e.g. caused by a power-up sequence, the entire digital design (including the ARM core, the bus-system and the APB peripherals) is reset to the initial state. A system reset has the same effect but retains the debug interface of the ARM

core, the SRAM content, and the state of the reset / wake-up status register. The information stored in the reset / wake-up register can be used by the software to distinguish between the different reset sources that caused the latest system reset.

4.7.4. Digital Watchdog (DWDG)

– 16-bit down counter

– Counter clock selectable

– Programmable trigger time

The digital watchdog module is used to supervise the program flow. A failure of the program flow that prevents retriggering the watchdog within a configurable time will generate a reset. The occurrence of the reset is stored in the reset status register and so the application SW can distinguish between a DWDG reset and any other reset source and thus react accordingly.

4.7.5. Window Watchdog (WWDG)

– Auxiliary 35 kHz oscillator as clock source

– Trigger window adjustable from 100 % to 0 % of the counter period

– Counter clock selectable

– Always enabled after reset, can be disabled by SW during initialization phase

The window watchdog module is used to supervise the program flow and the clocks generated by the main oscillator and the auxiliary oscillator. A failure of the program flow or an oscillator malfunction that prevents continuous triggering of the watchdog within a configurable time window will generate a reset. The occurrence of the reset is stored in the reset status register. By evaluating the reset status register the application SW can distinguish between a WWDG reset and any other reset source to react accordingly.

4.8. Peripherals

The HVC 5222C features several peripherals to offer an optimized solution for typical BLDC and BDC motor applications.

4.8.1. ADC

The ADC converts an analog input voltage in the range of 0 to 3.3 V into a 12-bit digital value including a sign bit. The reference voltage is derived from the internal band-gap.

– A/D converter with 12-bit data output (11 data bits + sign bit)
– Fast conversion time of 1 µs
– Multi-trigger feature with high priority (HP) and low priority (LP) selection
– Selectable trigger source for software-driven, event-driven, or time-dependent start of the acquisition queues
– High and low priority acquisition queues for automatic sequential acquisition of up to eight entries
– Programmable gain amplifier with five possible gain settings(x1, x2, x4, x8, x16).
– Individual interrupt sources for end of conversion (EOC) and trigger collision (TCOLL) for HP and LP queue

The acquisition queue holds up to eight entries and is executed after a defined start condition. The entries contain the input source and the gain setting. The converted values are stored in dedicated result registers. If all valid entries of the acquisition queue have been executed, an interrupt indicates the end of the conversion.

Table 4–6: ADC Multiplexer Table

Input	Mux	Reference	Range (V)	Gain	(1/LSB)	Function
BVDD	1	AVSS	6 to 18	1	19.34 mV	Supply supervision (R_{IN}~500 kΩ)
WAKE	2	AVSS	0 to 9.9	4	4.83mV	Motor phase voltage measurement e.g. for stall detection
MOUT2	3					
MOUT1	4					
MOUT0	5					
MVSS0	6	BVSS	-0.065 to 0.3	8	0.20 mV	External shunt measurement
MVSS1	7					
Temp	12			16	0.63 K	Junction temperature measurement
LIN BSM	13	BVSS	0 to 0.0129	16	11.0 uA	Internal bus-shunt voltage measurement with LIN BSM pre-amplifier gain of 16
LGPIO0	14	AVSS	0 to 3.3	1	1.61 mV	Single ended LGPIO measurement
LGPIO1	15					
LGPIO2	16					
LGPIO3	17					
LGPIO4	18					
LGPIO5	19					
LGPIO6	20					
LGPIO5	21	LGPIO6	-3.3 to 3.3*	1	1.61 mV	Pseudo-differential LGPIO measurement
*LGPIO input voltage specification must be observed.						

4.8.2. Enhanced PWM (EPWM)

The HVC 5221D features an enhanced PWM (EPWM) module for controlling the power bridge. It is optimized for BLDC, brush-type BDC and bipolar stepper motor control, supporting open-loop control modes (fixed voltage / fixed current) as well as closed-loop current control with a minimum amount of SW interaction.

– Control and diagnosis of the four half-bridges
– Support of BLDC, BDC and stepper motor control
– Support of mixed decay e.g. for stepper motor control
– Three EPWM control modules with programmable PWM period, PWM duty cycle and ADC trigger signal
– 12-bit EPWM counters for PWM generation in center- or edge-aligned mode
– Programmable PWM minimum on-time
– Current limit mode with PWM duty cycle capture
– Programmable slew rate for the half-bridges
– Optional buffering for the configuration registers

– Overcurrent and cross-current protection for each half-bridge
– Multiplexers to select control signals for high-side and low-side switches of each half-bridge (static at logical '0' or '1', inverted or non-inverted PWM signal)
– 3 interrupt lines, each triggered by end-of-period, compare, trigger, capture events of the corresponding EPWM control module or by an overcurrent event
– Dead-time insertion for operating 2 external P/N half-bridges

The internal PWM signals are generated by three independent EPWM control modules with separately programmable settings for the PWM period, PWM duty cycle and ADC trigger signal. Inside these modules there are multiplexers available to select the control signals for the high-side and low-side switches of each half-bridge and multiplexers to configure the EPWM module either in single half-bridge or paired half-bridge mode.

For system protection, the finite state machines inside the output control logic provide overcurrent and cross-current protection for each half-bridge.

4.8.3. Capture Compare Unit (CAPCOM)

– Processing of up to three channels in parallel
– 16-bit clock prescaler
– 16-bit free running CAPCOM counter
– 16-bit capture and compare registers for each channel
– Input capture event on rising, falling, or both edges
– Advanced capture mode with input pattern compare
– Optional buffering for configuration registers
– Three separately configurable output signals (static at logical '0', toggle on compare and/or overflow events)
– One interrupt line for each CAPCOM channel triggered by: overflow, compare, capture, capture overflow events; additional right / wrong pattern detection event for channel 0

The HVC 5222C features a capture-compare unit (CAPCOM) which is optimized to capture and process up to three channels in parallel, e.g. three hall sensor signals for sensor-based six-step BLDC motor control. In parallel the compare feature can be used to generate up to three output signals which are routed as alternative function to LGPIO ports.

4.8.4. TIMER

– Two timer modules: TIM0 and TIM1
– Selectable input clocks: internal or external
– 16-bit input clock prescaler
– 16-bit timer counter
– Selectable operating modes: timer, compare or capture
– Optional buffering of prescaler, reload- and capture values
– Selectable output signal: static value, PWM signal or timer input signal

The HVC 5222C features two instances of the timer module (TIM0, TIM1) with identical implementation which operate independently from each other. The timer modules are based on a 16-bit input clock prescaler and a 16-bit timer counter.

The timers can be used e.g. to generate periodic interrupts, to generate PWM output signals or to measure the pulse length of input signals.

4.8.5. LIN-UART

– ISO 17987 compliant data link layer
– Full duplex in non-LIN mode
– 8-bit frames
– Parity: none, odd or even
– One or two stop bits
– Programmable inverters at transmit output and receive input
– Baud rate pre-scaler: adjustment accuracy <0.5% (for entire LIN bit-rate range)
– Interrupts: transmitted, form error, parity error, transmit error, break or synch detected, RX FIFO not empty, RX/TX FIFO fill level reached, RX/TX FIFO overrun, TX FIFO empty, RX/TX FIFO full, TX frame end, TX frame end while TX FIFO fill level reached.
– Two independent 9-byte FIFOs for data reception and transmission
– Break/sync detection with automatic bit-rate adjustment in LIN mode
– Automatic LIN-header reception

The LIN-UART is a general purpose UART with enhanced features to unburden the CPU from LIN communication. It is a full duplex UART which can handle 8-bit telegrams with or without odd or even parity and one or two stop bits. The bit timing logic allows to adjust the necessary bit rate in small steps in order to synchronize to the LIN bit rate with a minimum residual error. Two 9-byte FIFOs are available for data reception and transmission. A bit-rate adjustment logic can be used for automatic adjustment of the UART bit rate to the bit rate of the LIN master. The enhanced features are optimized for the LIN slave mode.

The LIN-UART is compliant to the OEM requirement specification “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications v1.3” from May 4, 2012.

4.8.5.1. In-System Programming via LIN

The LIN pin can be used for in-system programming of the HVC 5222C flash. For detailed information see the corresponding Application Note “HVC 4x and HVC 5x Family – Boot Loader and Flash Programmer”, APN000129_004EN.

4.8.6. SPI

– 4-line interface (CSN, SCK, MISO, MOSI), full-duplex
– Master operation only
– Programmable bit rate from 78.125 kHz up to 2.5 MHz
– Programmable clock phase and polarity
– 8-, 16-, 24-, and 32-bit data frames supported by HW chip select (CSN)
– Chip Select (CSN) generation by HW or SW
– Programmable order of data bits (MSB or LSB first)
– Receive and transmit FIFOs with 8 × 8-bit each, organized according to the data frame width
– Interrupt generation at RX/TX events and FIFO flags

The SPI module provides a serial input and output link to external hardware, e.g. an EEPROM.

4.9. Memory

The HVC 5222C features several on-chip memory blocks to provide maximum flexibility for software development. A startup ROM takes care of system initialization and setting up of the program flow. For storing instruction code a flash memory is used whereas volatile application data are stored in the SRAM. An emulated EEPROM and NVR block can be used to store non volatile data.

4.9.1. Memory Map

The Arm® Cortex®-M3 provides a fixed linear memory map with 4 GB of addressable memory space. The internally predefined memory map specifies which bus interface is to be used when a memory location is accessed. In order to make it easier to port software, the registers of all internal peripherals, like Nested Vectored Interrupt Controller (NVIC), have a fixed position in the memory map.

4.9.2. Startup ROM

The HVC 5222C contains a startup ROM with the size of 1024 byte, organized as a 256-word by 32-bit array. It is used to store the start-up sequence which is executed after a reset, the default interrupt table and flash utility functions that can be used by the application SW. The memory content is fixed by design and cannot be reprogrammed in application.

4.9.3. Flash Memory with ECC

The HVC 5222C contains a flash memory which has the size of 32 KB and is organized as an 8192-word by 32-bit array. It is used to store the application SW and can be re-programmed in system. The flash can be programmed word by word, erasing is done either sector by sector or the complete flash memory. Sector size for erasing is 256 byte.

The flash memory is able to detect and to correct a single bit error within a 32-bit word. A double bit-error is detected during read of a 32-bit word. The error conditions are signalled in the flash status registers and can be configured as an interrupt source.

4.9.4. SRAM

The on-chip SRAM has the size of 2 KB and is organized as a 512-word by 32-bit array. It is used to store volatile application data, but can also be used to store and execute instruction code.

The content of the SRAM is preserved in ACTIVE, RETENTION, and OVERVOLTAGE mode but will be lost after power-down, THERMAL SHUTDOWN, and in SLEEP mode.

4.9.5. EEPROM with ECC

The emulated on-chip EEPROM has the size of 512 bytes and is organized as an 128-word by 32-bit array divided in 2 sectors with 256 byte each. The EEPROM array is used to store non-volatile application data like error counters or motor stop position.

The EEPROM memory is able to detect and to correct a single bit error within a 32-bit word. A double bit-error is detected during read of a 32-bit word. The error conditions are signalled in the flash status registers and can be configured as an interrupt source.

4.9.6. NVR with ECC

The on-chip NVR has the size of 256 bytes and is organized as an 64-word by 32-bit array. The NVR array is used to store non-volatile application data. It is not possible to program/erase NVR while reading the Program Flash. Thus, only a function running from SRAM or ROM can change the NVR.

The NVR memory is able to detect and to correct a single bit error within a 32-bit word. A double bit-error is detected during read of a 32-bit word. The error conditions are signalled in the flash status registers and can be configured as an interrupt source.

5. Document History

1. Data Sheet: HVC 5222C-B2 1 A Motor Controller for BLDC and BDC Motors with 32KB Flash and LIN", DSH000236_001EN, Nov. 16, 2023.
   First release of the Data Sheet. Changes to Advance Information AI000242_003EN are indicated by change bars.

Major Changes:

- Removed references to HVC 5223C.
- Removed LIN slew-rate specification from Section 3.5.1. on page 23 as this is not included in ISO17987.
- Corrected overvoltage behavior to include turn-off of MOUTx power stage.
- Increased operating current I_{DDP} by up to 2 mA in Section 3.5. on page 19.
- Widened AVDD spec to peak currents of up to 30 mA in Section 3.5. on page 19.

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